EDA Software for Verification of Metal Interconnects in ESD Protection Networks at Chip, Block, and Cell Level

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50 Words Abstract – A new EDA tool suite is presented for layout verification of ESD protection networks. It uses novel methodologies to accurately analyze interconnect resistance and current density, enabling quick identification of ESD weak areas at chip, block and detailed cell levels. The suite also includes a precision capacitance extraction tool.

I. Introduction

Metal interconnect layout is critical for ESD protection networks due to ever increasing IC complexity, shrinking ESD design window, increasing metal/via resistances in scaled technologies, and aggressive design schedules [1]. Even though the metal interconnect is a critical part of the ESD discharge path, it is often evaluated manually - which is error prone and tedious - or with tools not adequate for this analysis. In this paper we report a new methodology for verification of interconnects of ESD protection networks. This methodology is based on a suite including the following software tools, focusing on metal interconnect analysis:

- ESRA – for a block or full-chip level resistance and current density verification (explained in section II),
- R3D – for a detailed ESD cell level analysis (section III),
- F3D – for precise capacitance characterization (section IV).

A 28 nm process IP block was analyzed using a top-to-bottom approach, and potential weak areas were quickly identified. The initial analysis, performed at the top level (using ESRA), highlights problematic areas, which are further analyzed with a more detailed microscopic simulation approach (using R3D and F3D).

II. Full Chip / Block Level Analysis

When reviewing integration of proven ESD protection into the chip interconnect (see Fig. 1), ESD engineers need to be able to verify that there are low impedance / low current density paths between these protection elements and the external pads. For large and complex chips, manual reviews become difficult if impossible at all. Also, existing analysis tools are unable to handle metal interconnects information of large and complex chips without taking either too much time or too much compute resources.

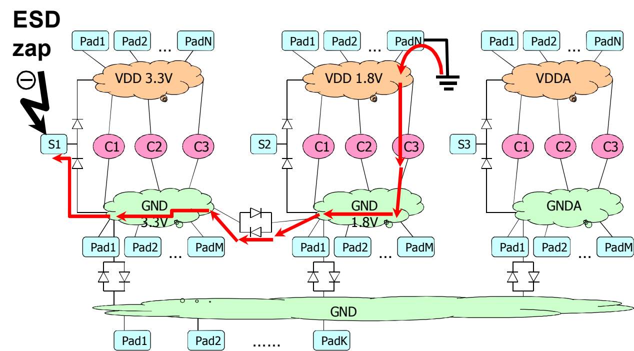

Figure 1: Diagram of ESD protection network and discharge path.

In this investigation, we consider a medium sized 28nm analog IP block that has an area of about 2x1 mm^2, 50 pads, and 11 metal layers. We examined the IP block to determine if any PAD to PAD discharge path interconnect has a resistance or a localized current density that exceeds our design specification. For this analysis we used ESRA (ESD Reliability Analyzer) which operates on a full chip or a block level layout, and performs the following checks:

1. Electrical connectivity of ESD network.
2. Resistance checks:
   a. pad-to-pad resistance for HBM / MM
   b. loop resistance for CDM events
   c. discharge path identification (pads / devices / nets)
3. Current density verification.

These checks are based on DC simulation of current flow in metal interconnects. While in real life ESD events involve transient effects, quite often the root causes of ESD failures are due to the problems of

metallization that can be captured using DC simulation. These kinds of issues concern too high resistive paths due to narrow metal lines, insufficient number of vias or contacts, poor connection of pads or ESD devices to ESD networks, etc.

It should be noted that even though DC simulation is a simpler problem than transient simulation, it is still a formidable problem if applied to ESD networks due to a huge size of the system, having a large number of small features and complex shapes. The huge size and complexity of the ESD network, and large number of ESD events that needs to be verified in an automated fashion, is the core task that ESRA is designed for. Another very important aspect of ESRA software is that while it helps analyze and debug huge layouts, it presents the data in formats that significantly speed up and simplify ESD network verification.

A diagram in Fig. 2 illustrates ESRA simulation flow.

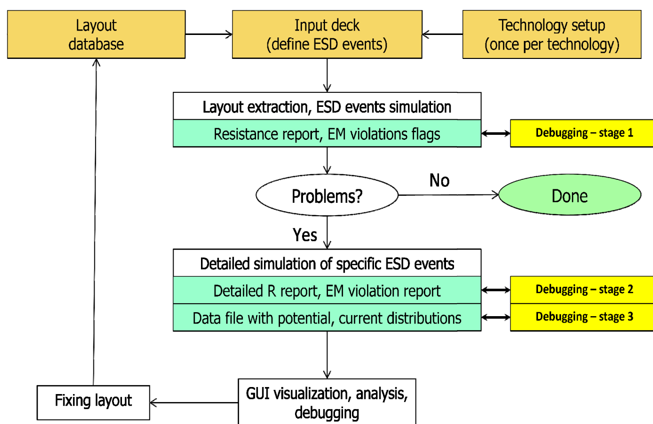

Figure 2: ESRA simulation flow.

ESRA input includes:

1. Layout (GDSII file or Calibre CI database)
2. Technology BEOL stacks description (in any of the industry standard formats).
3. ESD device definition.
4. Chip or package pads description.
5. ESD current density rules

Ease and intuitiveness of ESRA setup and use makes it useful for different groups of users: ESD and device engineers, circuit designers, and layout engineers.

ESRA performs a search for the minimum resistance path, starting from a zapped pad, going through electrically connected nets and ESD devices, finishing on a grounded pad or a group of grounded pads (Fig. 1). The tool handles the size and geometrical complexity of ESD networks by a "divide and conquer" approach that breaks the layout into tiles for geometry processing.

ESD devices are defined in the input deck by specifying ESD cell name, device type, differential resistance in forward and reverse directions, voltage drop, and a pair of pins (pin1, pin2) connecting the device ports to nets. An example of ESD device definition can be given as follows:

```
esd_dev DIODE pattern=esd28_ioclamp*
pin1=avss pin2=pad …
```

ESRA traces connectivity from these pins down to device terminal layers, to form a connected distributed resistive network for ESD devices and interconnects. Additional options of "esd_dev" command allow to specify multiple devices within the same cell, as well as to specify ESD devices present at the top level of hierarchy.

For CDM events, ESRA checks a "loop resistance" for a stressed pad, as illustrated in Figures 3 and 4. Analysis of a CDM event in even a relatively simple packaged die design can be an extremely complex problem because the charge is stored in a distributed fashion over the die and package (see Fig. 3). For a full solution, the whole integrated circuit and its package would need to be analyzed with a 3-D field solver to identify the distributed charge storage and the paths the discharge current takes during a CDM event. Currently, this kind of analysis is extremely computing expensive and the results may not be useful, depending on the assumptions made during the simulation setup or those made by the simulator.

To simplify the problem, the majority of the charge is assumed to be stored on the supply nets in the package and on the die. From a signal pad, the discharge current will be sourced from the supply or supplies to which the pad's ESD clamps are connected. As that supply charges or discharges, the supply clamps will trigger, equalizing potential between supplies. To protect the oxides of devices connected to the pad and to the supplies, the impedance of the path from the pad through the clamp (A in Figure 4), through the supply grid to the clamp or array of clamps (B in Figure 4), through the supply clamps (C in Figure 4) and back to the devices connected to the opposite supply (D in Figure 4) is mapped. If the total impedance is found to be too high, the trouble areas are easily identified and can be corrected before committing the design to fabrication.

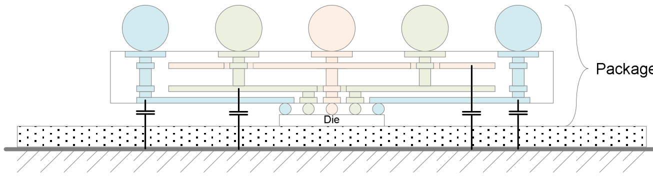

Figure 3: A cross section of a flip chip part on CDM test platform showing lumped capacitances to the visible nets. In reality, these capacitances are distributed over each net, both in the package and in the die.

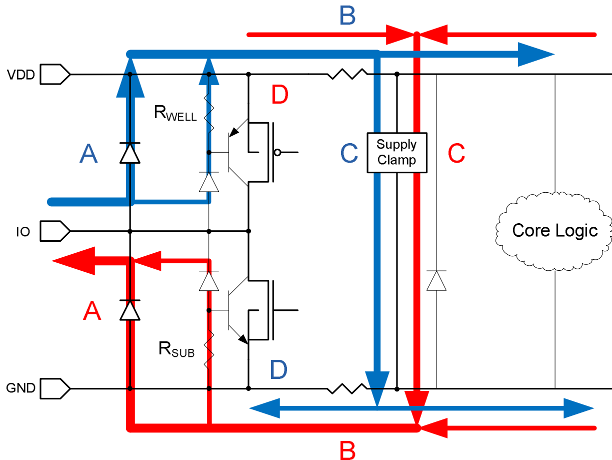

Figure 4: Idealized CDM discharge paths in a generic output driver with diode pad clamps. Here the blue path shows the current for a negatively charged part and the red path shows the current for a positively charged part. The resistors shown are the intrinsic resistance of the interconnect or diffusion.

“Coarse” top-level and detailed lower-level text and visual reports are generated (for HBM or CDM stress events, as specified by the user), helping to catch critical problems first, and then drill down in the layout to find what’s causing the failure.

Fig. 5 shows the top-level, pad-to-pad resistance report generated by ESRA and sorted by resistance and current density values. It also creates a database that is used for subsequent fast detailed analysis of critical ESD events. Using the coarse, top-level report allowed us to quickly identify the high risk nets.

hbm

File View Help

ID	NAME	V_[V]	I_[A]	R_[Ohm]
83	CORE_VDD_pos__1_AVSS_885_510.11_AP	1.609	1.3000	1.2380
84	CORE_VDD_neg__1_AVSS_885_510.11_AP	1.609	1.3000	1.2380
589	1P8_pos___CORE_VSS_1044.1_51.11_AP	1.577	1.3000	1.2134
590	1P8_neg___CORE_VSS_1044.1_51.11_AP	1.577	1.3000	1.2134
583	1P8_pos___CORE_VDD_248.6_142.91_AP	1.568	1.3000	1.2064
584	1P8_neg___CORE_VDD_248.6_142.91_AP	1.568	1.3000	1.2064
595	1P8_pos___CORE_VSS_407.7_51.11_AP	1.557	1.3000	1.1975
596	1P8_neg___CORE_VSS_407.7_51.11_AP	1.557	1.3000	1.1975
85	CORE_VDD_pos__1_AVSS_885_326.51_AP	1.552	1.3000	1.1942
86	CORE_VDD_neg__1_AVSS_885_326.51_AP	1.552	1.3000	1.1942
177	CORE_VSS_pos__1_AVSS_885_510.11_AP	1.545	1.3000	1.1885
178	CORE_VSS_neg__1_AVSS_885_510.11_AP	1.545	1.3000	1.1885
179	CORE_VSS_pos__1_AVSS_885_326.51_AP	1.488	1.3000	1.1446

Figure 5: Pad-to-pad resistance report sorted by values.

To speed up simulations, and to minimize the volume of generated data, the coarse report does not provide information on current densities and potential distributions. Thus, to investigate deeper the high resistance / current density path highlighted in Fig. 5 (negative HBM stress on pad AVSS vs. power group CORE_VDD), ESRA was run in detail on that path. The generated detailed report highlighting the criticality of various ESD path elements is shown in Figure 6. Criticality is defined in terms of resistance or magnitude of current density violation.

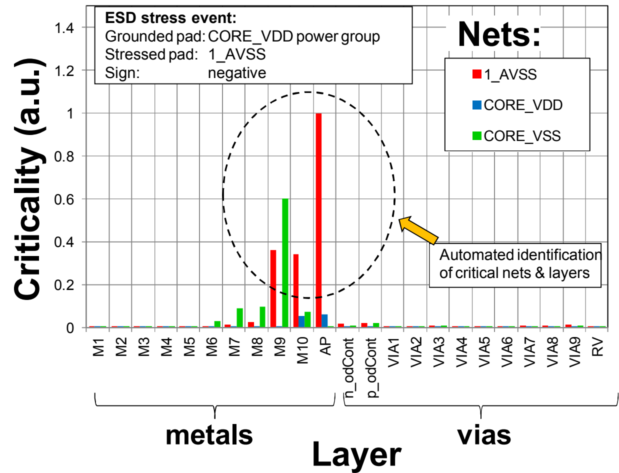

Figure 6: Detailed ESD event analysis highlighting the most critical layers.

This report helps immediately see what nets and layers have the largest impact on the resistance or current density violations. Based on the layers and nets identified in Figure 6, we viewed the corresponding visual reports (Figure 7 and 8) and quickly found the weak areas such as missing vias, narrow metals and a poor connection of the pads.

The total ESRA simulation time for this block was within 2 hours.

While these weaknesses were not enough to cause an easily identifiable single failure location, significant shifts in leakage after ESD stress verified that the overall power grid was compromised and this IP fails ESD.

In general, ESRA helps us in two different application areas:

1) For large IP blocks such as SERDES or audio codecs where the ESD protection network may not be planned in advance, and is put in as allowed after all the IP sub cells are placed. This results in a compromised power grid, from an ESD perspective. However, there is often a

considerable resistance from the IP team against redesigning their power grid. ESRA allows highlighting areas of the design that require improvement and gives the ESD design team a much more powerful argument to get those improvements implemented.

2) As a top level integration sign off tool. When many IP blocks from many internal and external IP vendors are integrated on one chip, one needs to have a tool that can contemplate ESD discharge paths from any charge injection point (pad) to any other charge extraction point. This would allow the integration team and the ESD team to verify that all ESD discharge paths are sufficient to support the project's ESD stress requirements.

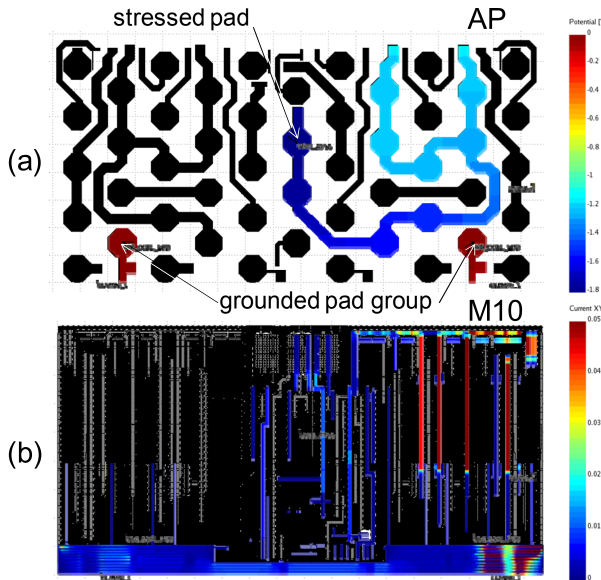

Figure 7: (a) Significant potential changes can be observed in layer AP and (b) current density issues in layer M10.

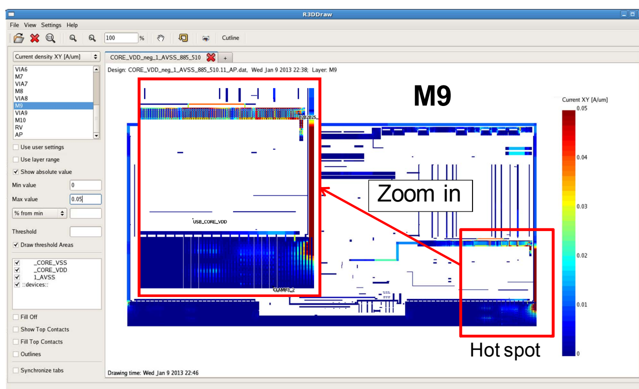

Figure 8: Visualization of the current crowding issues that were observed in the M9 layer.

III. ESD Device/Cell Interconnects

A design challenge ESD engineers face is the optimization of the interconnects in high current ESD discharge paths. While the optimum solution may be obvious, constraints can force significant deviations from the best implementation. The final solution is often based on general guidelines, best practices that may not even apply to the implementation, and guesswork.

While ESRA focused on large nets and long range effects, many high-current effects require a more detailed, localized simulation. We used R3D, a 3D mesh-based field solver for current flow simulation, to identify local trouble spots in an existing layout and to optimize diode interconnect in a new design.

R3D was originally developed to analyze large area power devices to accurately simulate current flow, voltage distributions and the device on-resistance with an emphasis on metal interconnects structure [2]. For that reason, it is well suited and very useful for analyzing ESD networks. It accounts for all details of the current flow, for example current crowding caused by sharp corners or slots, 2D and 3D current flow effects, distributed current flow in multi-finger devices, non-uniform current flow in multiple vias, and wide or mesh-like metal busses.

First Study: A 28nm Input Circuit

We used R3D to evaluate ESD diode performance for the same 28nm technology IP block that was discussed in the previous section. The investigated structure consists of a low-capacitance pad and an ESD diode. Figure 9 shows the layout of the structure (a) and the current density distributions in the interconnects (b) (c) (d). There is current crowding in AP (b) near the side of the C4 bump that is facing the diode and in the top edge corner of the VSS bus where the AP is routed from the chip to the structure. A non-uniform current distribution can be observed over the RV vias (c), with much higher current density in the RV vias in the middle of the pad (close to the M10 route) and in RV vias in the topmost edge of the VSS bus. A current crowding effect can also be observed at the sharp 90 degree corners of the M10 bus (d).

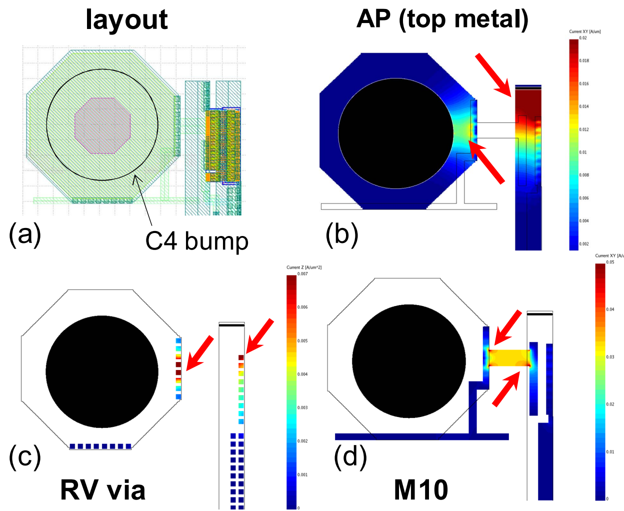

Figure 9: Layout and simulated current densities in the top metal layers and vias of an 28nm input circuit.

Figure 10 shows the current density in the diode and in selected metal and via layers. Current distribution over the diode area is strongly non-uniform, with higher current in the upper left corner. This is caused by the larger metallization resistance compared to the diode resistance. Layers M2 and Via9 exhibit non-uniform current distribution and high current densities in several areas such as the edge or corner vias and in the end of metal fingers.

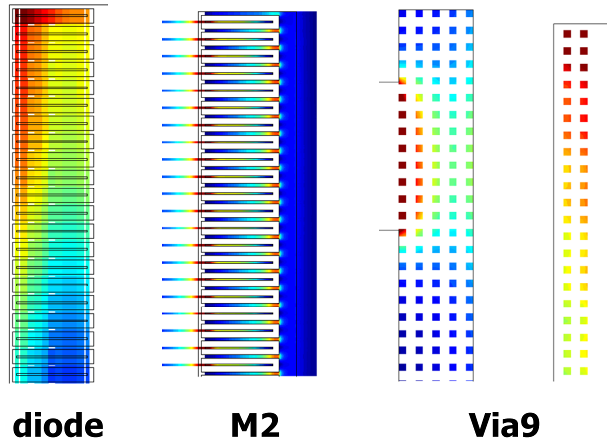

Figure 10: Current densities in selected layers over the top half of np-pw ESD diode (diode's active region, M2, and Via9). Two disjoint groups of Via9 belong to different diode terminals (anode and cathode).

This detailed information about the interconnect current flow and density provides the information necessary to analyze the efficiency of the interconnect in the ESD path. Also, it enables the design evaluation and optimization of the interconnect for optimum ESD performance.

R3D simulation time for these diodes was several minutes.

Second Study: A 55nm Diode Structure

In this example we are using R3D to analyze the interconnect of an ESD protection for a different design, fabricated in a 55 nm technology. A change in the overall chip integration of a product required the addition of stacked low voltage ESD diodes to an existing analog block with several layout and routing constraints. R3D was used to analyze the efficiency of ESD diode connection to the protected nets, an to optimize metal interconnects for current density and resistance.

Three metal layers are available for the ESD structure, with VSS and VDD busses implemented horizontally. The layout configuration easiest to plug into the existing analog IP has both ESD device terminals on the same side. A parallel configuration of the current flow (terminals on the opposite sides) and trapezoidal metal shapes, which are well known to result in a much more uniform current distribution, required a significant change in the analog IP layout. R3D was used to determine if the cost of modifying the analog IP was worth the benefit in the ESD performance. Figure 11 shows the current density in M3, while Figure 12 shows the current density in the diodes simulated for different layout options. In case (a), due to a high resistance of M3 layer, there is a significant voltage drop (metal debiasing) on the M3 routes and the current density decreases linearly along the diode. The parallel configuration results in a much more uniform current distribution over the device area (case (b)). Trapezoidal metal shapes give the lowest current density in M3 and the most uniform current distribution in the diodes (case (c)). Based on these results, the implementation best suited for the investigated application can be chosen. Calculated resistances were: (a) R=2.51 Ohm, (b) 2.50 Ohm, and (c) R=1.94 Ohm.

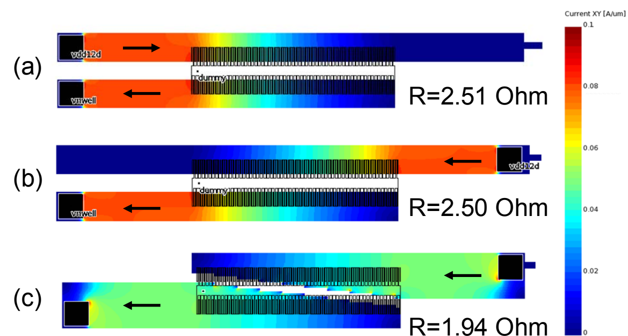

Figure 11: M3 current densities in layouts with (a) ports located on the same side, (b) on opposite sides, and (c) trapezoidal metals.

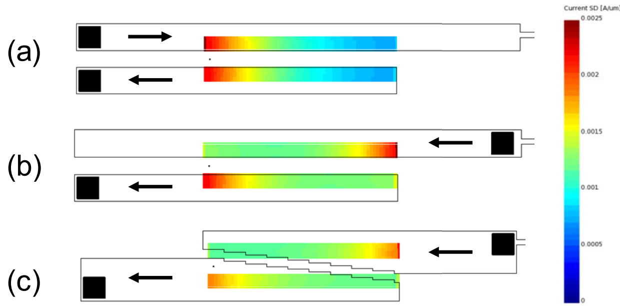

Figure 12: Simulated current densities in the diodes.

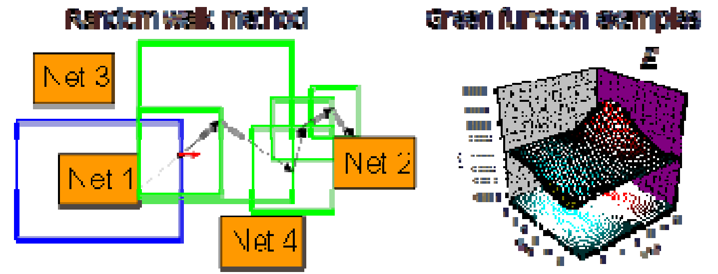

Figure 13: Schematic illustration of random walk method, and surface Green function for the electric field.

IV. Capacitance Minimization

One of the constraints ESD engineers must juggle while designing the ESD discharge path interconnect is the need to keep signal pad interconnect capacitance as low as possible [3]. This is particularly true for high speed and RF IOs where the ESD discharge path interconnect and clamp devices often contribute the majority of the parasitic capacitive load. R3D can show us the metals and vias that carry only a small fraction if any of the current and that may be trimmed or removed. However, we need accurate information about the total capacitance and the contributions from the different components of the interconnects to know where to make optimizing modifications. Also, since capacitance changes from metal interconnect layout modifications can be small (e.g. 5%), high accuracy (1% or better) extracted capacitance is required to correctly predict trends and find the optimum design point.

To help us identify optimization candidate areas in order to achieve a low-capacitance IO design (analyzed in sections II and III), we used F3D, a capacitance and RC extraction software tool based on a floating random-walk method [4]. Random walk method is a statistical (Monte Carlo) technique used for solving deterministic partial differential equations. This method offers a unique opportunity to achieve a rigorous, first principles, solution of the capacitance problem, with a minimum of simplifying assumptions.

Capacitance is calculated as an integral of contributions from many random walks that start on a Gaussian surface around a net, and end up on other nets. Random walk trajectory properties are defined by the Green functions of the Laplace equation for the "cubes" computed for each hop (see Fig. 13 and Fig. 14).

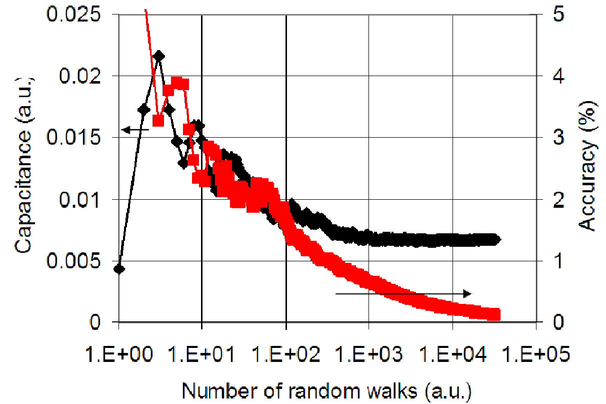

Figure 14: Illustration of capacitance convergence and error reduction with increase of number of random walks.

A 3D view of the low-capacitance pad is shown in Figure 15. This pad is connected to the ESD diode (analyzed in the previous section) within the same IP block that was discussed in section II. A 3D view generated by F3D can be interactively visualized. This helps visually understand the 3D geometry, and can provide some insight into capacitive effects, since capacitance is very closely related to the geometry.

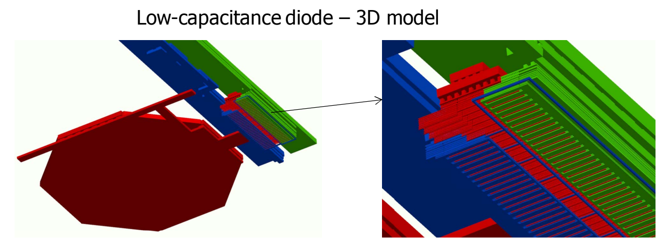

Figure 15: A 3D view of the low-capacitance pad.

The calculated total and coupling capacitances are reported in Table 1. Total simulation time was several minutes for accuracy of 1% (on one CPU).

Table 1: calculated capacitance components of pad.

Total	Coupling			
pad	VDD	VSS	GND	other
270 fF	64 fF	92 fF	100 fF	14 fF

Contributions of different metal layers to the total pad capacitance are shown as a Pareto plot in Figure 16. The largest contribution is coming from the top layers - AP (pad) and M10. Metals M1-M6 contribute ~4%-8% each, and contributions from layers M7-M9 are less than 3%. This is very useful practical information, as it helps to identify the most critical layers, to quantify their contributions, and to understand what nets they are coupled to. Along with DC current simulation results offered by R3D software (see section III), F3D provides a framework for comprehensive analysis and optimization of low-capacitance pads and low capacitance ESD devices.

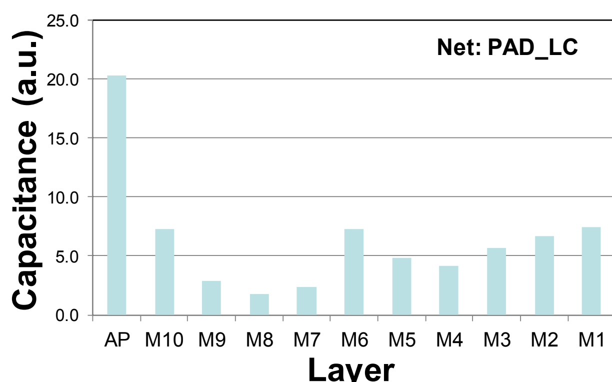

Figure 16: Individual metal layers contributions (in percents) to total pad capacitance.

V. Conclusions

To optimize the interconnects of ESD devices and networks, a new suite of tools was used that performs electrical simulation and is capable of analyzing large complex metal interconnects. ESRA performs a block or full chip level connectivity, resistance, and current density checks. R3D enables a detailed, microscopic analysis and simulation at the ESD cell or small block level. F3D provides high-precision calculation of parasitic interconnects capacitance, to help optimize low-capacitance designs. Current flow in the ESD paths, current density, ESD path resistances, general connectivity, and the capacitance of ESD device interconnects were analyzed and optimized. ESD network problems could be captured and fixed early in the design phase. Ease of setup and use of these tools significantly reduces a barrier for a new tool adoption by a diverse group of users – ESD engineers, device engineers, and layout and circuit designers.

References

[1] ESD Association, "ESD Electronic Design Automation Checks", Report TR18.0-01-11, 2012.

[2] M. Ershov et al., "Numerical Simulation of Metal Interconnects of Power Semiconductor Devices", Proc. ISPSD 2010, pp. 185-188.

[3] M.-D. Ker, and Y.-W. Hsiao, "ESD Protection Design With Low-Capacitance Considerations for High-Speed / High-Frequency I/O Interfaces in Integrated Circuits", Recent Patents on Engineering, v. 1. No.2, p. 131, 2007.

[4] Y. L. Le Coz and R. B. Iverson, "A Stochastic Algorithm for High Speed Capacitance Extraction in Integrated Circuits", Solid State Electronics, v. 35, no. 7, pp. 1005-1012, 1992.